IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

BOARD OF PATENT APPEALS AND INTERFERENCES

Applicant:	Mark T. McCORMACK, et al.
Serial No.:	**09/866,092**
Filed:	May 23, 2001
For:	*Structure and Method of Embedding Components in Multi-Layer Substrates*
Group Art Unit:	2815
Examiner:	Eugene LEE
Confirmation No.:	5484

APPLICANT'S APPEAL BRIEF UNDER 37 C.F.R. § 41.37

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I. REAL PARTY IN INTEREST

The present application is owned by Fujitsu Limited, a Japanese Corporation.

II. RELATED APPEALS AND INTERFERENCES

None.

III. STATUS OF CLAIMS

Claims 1 – 16, 25 and 35 have been cancelled.

Claims 17 – 24, 26 – 34 and 36 – 44 stand rejected.

Appeal is taken as to all of the rejected claims.

IV. STATUS OF AMENDMENTS

No amendment has been filed subsequent to the rejection from which this appeal is taken.

V. SUMMARY OF CLAIMED SUBJECT MATTER[1]

Generally, the present invention is related to multi-layer substrates, and in particular to a circuit apparatus and a method for embedding electronic components within multi-layer substrates, such as printed circuit boards, that is cost-effective and efficient.

Independent Claim 17 is directed to a multi-layer printed circuit board having at least one prefabricated, integrated electronic component embedded therein, where the core of the multi-layer printed circuit board is a polymeric circuit board substrate with first and second surfaces (Specification as filed, page 3, lines 2 – 4, page 7, lines 2 – 4, ref. nos. 10, 12, 12a, and 12b in Fig. 1, and ref. no. 20 in Fig. 3). An integrated electronic component is prefabricated prior to being securely attached in a cavity in the first surface of the polymeric substrate (page 3, lines 4 – 6, page 7, lines 26 – 30, ref. no. 20 in Figs. 3 and 13 and ref. no. 24 in Fig. 12). A dielectric layer is disposed on the first substrate surface and over the integrated electronic component, and a metallic layer is disposed on the dielectric layer (page 3, lines 5 – 7, page 8, lines 13 – 21, ref. nos. 30 and 32 in Fig. 4, and ref. nos. 40 and 42 in Figs. 5 and 6). An electrically conductive via passes through the dielectric layer in contact with the metallic layer and a second dielectric layer

[1] The summary characterizations of the claimed inventions set forth below are not intended as rigorous interpretations of any of the claims, and the failure to mention certain claimed features in this introductory discussion is not intended to suggest that such features are unimportant for purposes of patentability.

is disposed over the via and the metallic layer (page 3, lines 8 – 10, page 8, lines 12 – 15 and 22 – 31, ref. nos. 46 and 50 in Fig. 6, and ref. nos. 60 and 64 in Fig. 8). A second electrically conductive via extends at one location through the first and second dielectric layers and is electrically coupled to the integrated electronic component (page 3, lines 10 – 12, page 8, lines 16 – 19, and ref. no. 70 in Fig. 9).

Dependent Claims 18 – 24, 26 – 34 and 36 – 39 specify additional features of the multi-layer circuit board, such as additional metallic layers, multiple polymeric layers comprising the core substrate, patterning of the metallic layers, a second integrated electronic component, and a capacitor comprising the integrated electronic component.

Independent Claim 40 is directed to a multi-layer printed circuit board, where the core of the multi-layer printed circuit board is a polymeric circuit board substrate, having a prefabricated capacitor disposed in a cavity in the substrate, where the capacitor has a contact pad (page 3, lines 2 – 6, page 7, lines 2 – 4 and 26 – 30, page 8, lines 1 - 5, ref. nos. 10 and 12 in Fig. 1, ref. nos. 20 and 26 in Fig. 3, and ref. no. 24 in Fig. 12). A dielectric layer is disposed on the substrate and over the capacitor, and a metallic layer is disposed on the dielectric layer (page 3, lines 5 – 7, page 8, lines 13 – 21, ref. nos. 30 and 32 in Fig. 4, and ref. nos. 40 and 42 in Figs. 5 and 6). An electrically conductive via passes through the dielectric layer in contact with the contact pad and a second dielectric layer is disposed over the via and the metallic layer (page 3, lines 8 – 10, page 8, lines 12 – 15 and 22 – 31, ref. nos. 46 and 50 in Fig. 6, and ref. nos. 60 and 64 in Fig. 8). A second electrically conductive via extends at one location through the first and second dielectric layers and is electrically coupled to the capacitor (page 3, lines 10 – 12, page 8, lines 16 – 19, and ref. no. 70 in Fig. 9).

Dependent Claims 41 – 43 specify that the multi-layer printed circuit board is comprised of pluralities of cavities and capacitors, that the capacitor comprises a petrovskite capacitance material, and that the capacitor is fabricated at a temperature higher than the maximum processing temperature of the circuit board.

Independent Claim 44 is directed to a multi-layer printed circuit board, where the core of the multi-layer printed circuit board is a polymeric circuit board substrate with opposing first and second sides, having a prefabricated electronic component disposed in a cavity in the first side of the substrate, where the prefabricated electronic component has a contact pad (page 3, lines 2 –

6, page 7, lines 2 – 4 and 26 – 30, page 8, lines 1 – 5, ref. nos. 10 and 12 in Fig. 1, ref. nos. 20 and 26 in Fig. 3, and ref. no. 24 in Fig. 12). A dielcctric layer is disposed on the first side of the substrate and over the prefabricated electronic component, and a metallic layer is disposed on the dielectric layer (page 3, lines 5 – 7, page 8, lines 13 – 21, ref. nos. 30 and 32 in Fig. 4, and ref. nos. 40 and 42 in Figs. 5 and 6). An electrically conductive via passes through the dielectric layer in contact with the contact pad and a second dielectric layer is disposed over the via and the metallic layer (page 3, lines 8 – 10, page 8, lines 12 – 15 and 22 – 31, ref. nos. 46 and 50 in Fig. 6, and ref. nos. 60 and 64 in Fig. 8). A second electrically conductive via extends at one location through the first and second dielectric layers (page 3, lines 10 – 12, page 8, lines 16 – 19, and ref. no. 70 in Fig. 9). A third dielectric layer is disposed on the second side of the substrate and a patterned metallic layer is disposed on the third dielectric layer (page 9, lines 12 – 30, and ref. nos. 32, 94 and 98 in Fig. 9).

There are no "means-plus-function" or "step-plus-function" claim elements under 35 U.S.C. § 112, sixth paragraph, in any of the claims.

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

The rejection to be reviewed is from the Final Office Action dated July 6, 2006, from which the present appeal is taken. Because the present application has been rejccted at least twice, appeal from the July 6, 2006, Final Office Action is appropriate under 35 U.S.C. § 134 and 37 C.F.R. § 41.31.

Rejections under 35 U.S.C. § 103

Claims 17, 38 and 39 were rejected as obvious over **Ma et al.** (U.S. Patent No. 6,154,366) in view of **Saito et al.** (U.S. Patent No. 5,049,980) in view of **Cole, Jr. et al.** (U.S. Patent No. 5,073,814).

Claims 17, 18, 20 – 23, 27, 30, 36, 38 – 41 and 43 were rejected as obvious over **Miura et al.** (U.S. Patent No. 5,565,706) in view of **Saito et al.** in view of **Cole, Jr. et al.**

Claim 19 was rejected as obvious over **Miura et al.** in view of **Saito et al.** in view of **Cole, Jr. et al.**, and further in view of **Desai** (U.S. Patent No. 5,739,188).

Claims 24, 26, 28, 29, 31, 32 and 44 were rejected as obvious over **Miura et al.** in view of **Saito et al.** in view of **Cole, Jr. et al.**, and further in view of **Marcinkiewicz et al.** (U.S. Patent No. 5,241,456).

Claims 33 and 34 were rejected as obvious over **Miura et al.** in view of **Saito et al.** in view of **Cole, Jr. et al.**, and further in view of **Ma et al.**

Claims 37 and 42 were rejected as obvious over **Miura et al.** in view of **Saito et al.** in view of **Cole, Jr. et al.**, and further in view of **Miyazawa et al.** (U.S. Patent No. 5,953,619).

VII. ARGUMENT

A. Introduction

All of the pending claims of this application were rejected as obvious over various combinations of Ma et al. (U.S. Patent No. 6,154,366), Miura et al. (U.S. Patent No. 5,565,706), Saito et al. (U.S. Patent No. 5,049,980), Cole, Jr. et al. (U.S. Patent No. 5,073,814), Desai (U.S. Patent No. 5,739,188), Marcinkiewicz et al. (U.S. Patent No. 5,241,456), and Miyazawa et al. (U.S. Patent No. 5,953,619). To establish a prima facie case of obviousness, all of the claim limitations must be taught or suggested by the prior art. *In re Royka*, 490 F.2d 981, 180 USPQ 580 (CCPA 1974). M.P.E.P. § 2143.03. Additionally, an examiner must show more than the presence of the elements of a claim in a collection of prior art references. The examiner must also show some suggestion or motivation for making the combination. *In re Bond,* 15 USPQ2d 1566 (Fed. Cir. 1990); *Carella v. Starlight Archery and Pro Line Co.,* 804 F.2d 135, 140, 231 USPQ 644, 647 (Fed. Cir. 1886); *see also ACS Hosp. Sys., Inc. v. Montefiore Hosp.,* 732 F.2d 1572, 1577, 221 USPQ 929, 933 (Fed. Cir. 1984).

B. The Rejection of Claims 17, 38 and 39 as obvious over Ma et al. in view of Saito et al. in view of Cole, Jr. et al.

1. Claim 17

a. *Ma et al. does not teach an integrated electronic component attached in a cavity in the substrate surface.*

Ma et al. teaches a microelectronic die package that is moisture resistant. The reference merely shows an IC chip that is mounted on a flexible wiring interconnect, referred to in the patent as a "flex component." The chip is then encapsulated with an encapsulant, and additional

wiring layers may be added onto the flex component. Ma et al. is principally directed to the use of moisture barriers surrounding the chip. Ma et al. does not show a cavity formed in a core substrate in which a prefabricated component is mounted. On the contrary, in Ma et al., a component is surrounded, after having already been connected to a substrate, with an encapsulating material. This technique is much different than securing a prefabricated component in a cavity that has been pre-formed in a substrate.

Although the Examiner stated in the rejection that Ma et al. teaches a cavity (Office Action dated July 6, 2006, page 2), there is no indication of any portion of the reference, either the text or the figures, that teaches that feature. With regard to the Examiner's Response to Arguments (Office Action dated July 6, 2006, page 8), where the Examiner stated that "[t]he claim only states structurally a core wherein the core is polymeric," the Applicant respectfully disagrees. Lines 5 – 6 of Claim 17 claim the feature of a first integrated electronic component securely attached in a cavity, therefore this feature must be addressed in a rejection of the claim.

In addition, Applicant strenuously disagrees with the Examiner's statement that page 10 of the Specification "states that the core need only be made of polymeric compounds, etc.," (Office Action dated July 6, 2006, page 8). Page 10 of the Specification provides information about the types of materials that may be suitable for use in the various components of the disclosed device, but there is no discussion related to any structural limitations of the core substrate. Applicant notes that even if a structural limitation had been discussed, it would have been improper for the Examiner to read such limitation into the claims (*see* MPEP § 2111.01). Finally, with respect to the Examiner's comment about the limiting effects of the preamble (Office Action dated July 6, 2006, page 8), the Examiner has not indicated to which argument this is intended to respond, as is required under § 707.07(f) of the MPEP, and Applicant is unable to determine how the Examiner's statement is relevant to the arguments discussed.

b. *Cole, Jr. et al. does not teach a second electrically conductive via extending* at one location *through the first and second dielectric layers.*

Having acknowledged that Ma et al. in view of Saito et al. does not teach a second electrically conductive via extending at one location through the first and second dielectric layers, the Examiner has relied upon Cole, Jr. et al. for that element. However, Applicant respectfully disagrees with the Examiner's interpretation of the reference. Cole, Jr. et al.

discloses a multi-sublayer dielectric layer (ref. no. 20 in Figs. 1 and 2) that is comprised of sublayers of a polyimide material (ref. no. 24) and a fluoropolymer (ref. no. 26) and a thermoplastic adhesive sublayer (ref. no. 22). The alternating sublayers are bonded to a substrate with the adhesive sublayer, then the via holes (ref. no. 28) are drilled through the entire dielectric layer and the dielectric layer is coated with the metal layer (ref. no. 30). The reference specifically states that "the entire stack of sublayers 24 and 26 along with the adhesive sublayer form a single dielectric layer 20," (col. 10, line 68 – col. 11, line 2). Thus, Cole, Jr. et al. merely teaches a via that goes through a *single* dielectric layer, regardless of the variations in the composition of that layer. This is in direct contrast with the claimed invention.

The relevant portion of Claim 17 requires a first dielectric layer, over which a metallic layer is disposed, a second dielectric layer disposed over the metallic layer, and a second via extending at one location through both the first and second dielectric layers. Thus, the dielectric layers are separated by the metallic layer, and the second via extends through the entire stack. The structure in Cole, Jr. et al. that actually has *two* dielectric layers is shown in Fig. 2, where it can be seen that there is *no* via that extends *at one location* through both the first and second dielectric layers. This interpretation of the reference is further supported by the reference's own definition: "The term 'dielectric layer' is used to identify that dielectric material which is disposed between two different levels of conductors," (col. 10, lines 65 – 67). Accordingly, Cole, Jr. et al. teaches offset or staggered vias, but not a via as claimed in Claim 17 of the present application.

c. *The combination of Ma et al. and Saito et al. with Cole, Jr. et al. was improper.*

The Examiner asserted as the motivation to combine Cole, Jr. et al. with Ma et al. and Saito et al. that it would have been obvious "in order to lessen manufacture time by laying down one layer instead of multiple layers," (Office Action dated July 6, 2006, page 3). It is unclear to what "layers" the Examiner intended to refer, possibly the metallic layers. Regardless, this rationale appears contrary to the teachings of Cole, Jr. et al., which specifically involves the layering of multiple layers and sublayers of various types, such as the polyimide sublayers (ref. nos. 24 and 44 in Fig. 2), the fluoropolymer sublayers (ref. nos. 26 and 46 in Fig. 2), the thermoplastic adhesive sublayers (ref. nos. 22 and 42 in Fig. 2) and the metal layers (ref. no. 30 in Fig. 1 and ref. no. 50 in Fig. 2). Further, Ma et al. expressly discloses that additional layers of

flex components and conductive traces can be attached on top of each other (col. 3, lines 19 – 23). As cited above, the Examiner must show some motivation or suggestion for the combination, which he has not done. The Examincr has not shown that there is any suggestion that a single layer would be preferable to multiple layers, nor any other indication in the references or in the art that such a combination would be desirable. Accordingly, it is submitted that the Examiner has not shown a proper basis for combining the references.

Therefore, because Ma et al. in view of Saito et al. and Cole, Jr. et al. does not teach several of the claimed elements of the present invention and it would not have been obvious to combine Ma et al. and Saito et al. with the teachings of Cole, Jr. et al., Applicant respectfully submits that the subject matter of Claim 17 was not obvious, and the claim was not properly rejected.

2. Claims 38 and 39

Claims 38 and 39 depend from independent Claim 17 and thus were not properly rejected for at least the same reasons.

C. The Rejection of Claims 17, 18, 20 – 23, 27, 30, 36, 38 – 41 and 43 as obvious over Miura et al. in view of Saito et al. in view of Cole, Jr. et al.

1. Claims 17 and 40

a. *Miura et al. does not teach a polymeric core substrate nor would it have been obvious to use a polymeric core substrate in the device of Miura et al.*

Claims 17 and 40 specify that the core substrate is "polymeric;" however, all of the embodiments discussed in Miura et al. use ceramic or silicon core substrates. Polymers are only used in Miura et al. for purposes other than as a core substrate. Although the Examiner acknowledges this deficiency in Miura et al. and relies upon Saito et al. for the teaching of a polymeric substrate, the Examiner has failed to provide motivation for the combination. Additionally, the Examiner has failed to respond to Applicant's previous argument that the reference, as well as general knowledge in the art, teaches away from substituting a polymeric core substrate for the ceramic substrate in Miura et al. Instead, the Examiner provided a general statement that motivation need not be expressly articulated and concluded that it would have been obvious to one of ordinary skill in the art to makc such a substitution (Office Action dated July 6, 2006, page 8).

In contrast to the Examiner's assertion, it would not have been obvious to one of ordinary skill in the art to substitute a polymeric substrate for the substrate in Miura et al. First, Miura et al. specifically differentiates ceramic substrates from polymeric substrates, for example in its discussion of related art where the differences between ceramic wiring boards and polymeric wiring boards are detailed (*see* col. 1, line 20 – col. 2, line 58). It is clear from this discussion in Miura et al. that the two are not considered interchangeable. One important difference between the ceramic and polymeric substrates is their respective thicknesses. The ceramic substrates disclosed in Miura et al. are 0.8 mm (800 microns) thick (col. 8, lines 11 – 12), whereas the polymeric layers disclosed in the present application are 40 microns thick – *i.e.*, 5 % of the ceramic substrate thickness. In addition, ceramic processing technology is quite different that polymeric processing technology. Because of the significant size and processing differences between these two technologies, persons of skill in the art do not view them as interchangeable. The Examiner's mere statement that a resin substrate, as disclosed in Saito et al., is known to be more flexible and less likely to break than ceramic, and that this provides motivation to combine the two references ignores the substantial reasons why one of ordinary skill in the art would *not* combine the references.

b. *Cole, Jr. et al. does not teach a second electrically conductive via extending* at one location *through the first and second dielectric layers.*

In a manner similar to the rejection of Claim 17 as obvious over Ma et al. in view of Saito et al. and Cole, Jr. et al., the Examiner acknowledged that Miura et al. in view of Saito et al. does not teach a second via as claimed in Claim 17 and relied upon Cole, Jr. et al. for that element. As discussed above, Cole, Jr. et al. teaches offset or staggered vias, but does not teach a second electrically conductive via that extends at one location through the first and second dielectric layers.

Therefore, because Miura et al. in view of Saito et al. and Cole, Jr. et al. does not teach all of the claimed elements of the present invention and it would not have been obvious to substitute the substrate of Saito et al. for that in Miura et al., Applicant respectfully submits that the subject matter of Claims 17 and 40 was not obvious, and the claims were not properly rejected.

2. Claims 36, 40, 41 and 43

Claims 36, 40, 41 and 43 all require that prefabricated capacitors be incorporated into cavities formed in polymeric core substrates. None of the prior art of record relied upon by the Examiner shows capacitors secured in cavities in polymeric substrates. Accordingly, Applicant submits that Claims 36, 40, 41 and 43 were not properly rejected.

3. Claims 18, 20 – 23, 27, 30, 36, 38, 39, 41 and 43

Claims 18, 20 – 23, 27, 30, 36, 38 and 39 depend from independent Claim 17 and Claims 41 and 43 depend from independent Claim 40 and were improperly rejected for at least the same reasons.

D. The Rejection of Claim 19 as obvious over Miura et al. in view of Saito et al. in view of Cole, Jr. et al., and further in view of Desai

Claim 19 depends from independent Claim 17 and was improperly rejected for at least the same reasons.

Additionally, the Examiner has not shown sufficient motivation to combine the Desai reference with Miura et al, Saito et al. and Cole, Jr. et al. First, Desai is in a wholly different art than the references with which it has been combined. Desai teaches a thermoplastic polymer compound and a method of processing that compound. It does not relate to the formation or processing of polymeric substrates for circuit boards or even to the field of electronic components generally, nor does the reference provide that any of its teachings may be applicable to the formation of a circuit board. Desai is primarily concerned with improving the processing stability of thermoplastic polymers and improving their flow characteristics. There is no indication that the problems addressed by Desai have any relation to those in Miura et al., Saito et al. or Cole, Jr. et al. or to the present application.

Second, the Examiner has stated as the motivation to combine these references the protection of the substrate (Office Action dated July 6, 2006, page 5). However, the Examiner has provided no support for that line of reasoning. While it is true that the motivation to combine references need not be *explicitly* stated, there must be some basis in the references or the art as a whole that provides a teaching, suggestion or motivation to combine. Here, Desai teaches a multi-layered polymer product where a core layer is covered by a cap layer not for the protection of the core layer, as suggested by the Examiner, but to hide the imperfections in the

core layer (Desai, col. 3, lincs 26 – 37). Similarly, there is no teaching in any of the references with which Desai was combined that suggests the motivation citcd by the Examiner.

Accordingly, Applicant asserts that without some indication of why one of ordinary skill in the art would look to the field of Desai and use the teachings of Desai with those of Miura et al., Saito et al. and Cole, Jr. et al., these references have been improperly combined, and thus Claim 19 was not properly rejected.

E. The Rejection of Claims 24, 26, 28, 29, 31, 32 and 44 as obvious over Miura et al. in view of Saito et al. in view of Cole, Jr. et al., and further in view of Marcinkiewicz et al.

1. Claims 24, 26, 28, 29, 31 and 32

Claims 24, 26, 28, 29, 31 and 32 depend from independent Claim 17 and were improperly rejected for at least the same reasons.

2. Claims 31 and 32

Claims 31 and 32 require at least one metal-lined via extending through the metallic layer and the first dielectric layer. On page 7 of the Office Action dated July 6, 2006, the Examiner stated that this fcature was not taught by the combination of Miura et al., Saito et al. and Cole, Jr. et al. (in the paragraph rejecting Claims 33 and 34). In the rejection of Claims 31 and 32, the Examiner did not identify any teaching in Marcinkiewicz et al. that cures this deficiency and there is no such teaching. Accordingly, Applicant asserts that the features of Claims 31 and 32 were not taught by Miura et al., in view of Saito et al., Cole, Jr. et al. and Marcinkiewicz et al. and therefore the claims were not properly rejected.

3. Claim 44

As discussed above with respect to Claims 17 and 40, Miura et al. does not teach a polymeric core substrate nor would it have been obvious to use a polymeric core substrate in the device of Miura et al. Because the ceramic substrate of Miura et al. and the polymeric substrate of Saito et al. are not considered interchangeable in the art, it would not have been obvious to one of ordinary skill in the art to substitute a polymeric substrate for the substrate in Miura et al. Also as discussed above, Cole, Jr. et al. does not teach a second electrically conductive via extending *at one location* through the first and second dielectric layers. Cole, Jr. et al. teaches offset or staggered vias, but does not teach a via as claimed in Claim 44.

Therefore, because Miura et al. in view of Saito et al. and Cole, Jr. et al., and further in view of Marcinkiewicz et al. does not teach all of the claimed elements of the present invention and it would not have been obvious to substitute the substrate of Saito et al. for that in Miura et al., Applicant respectfully submits that the subject matter of Claim 44 was not obvious, and the claim was not properly rejected.

F. The Rejection of Claims 33 and 34 as obvious over Miura et al. in view of Saito et al. in view of Cole, Jr. et al., and further in view of Ma et al.

Claims 33 and 34 depend from independent Claim 17 and were improperly rejected for at least the same reasons.

G. The Rejection of Claims 37 and 42 as obvious over Miura et al. in view of Saito et al. in view of Cole, Jr. et al., and further in view of Miyazawa et al.

Claim 37 depends from independent Claim 17 and Claim 42 depends from independent Claim 40 and were improperly rejected for at least the same reasons.

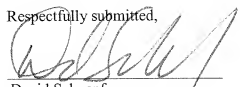
Additionally, Claims 37 and 42 both require that prefabricated capacitors be incorporated into cavities formed in polymeric core substrates. None of the prior art of record relied upon by the Examiner shows capacitors secured in cavities in polymeric substrates. Further, Claims 37 and 42 specify that the capacitors comprise a petrovskite capacitance material. The Examiner has failed to show sufficient motivation for combining the teachings of Miura et al., Saito et al. or Cole, Jr. et al. with Miyazawa et al. The Examiner has merely asserted that it would have been obvious to one of ordinary skill in the art to use a petrovskite capacitanee material in order to provide a higher dielectric constant. However, this statement does not provide any explanation as to why one would find it obvious to incorporate a material with such a dielectric constant into the device of Miura et al. Accordingly, Applicant asserts that the subject matter of Claims 37 and 42 was not obvious in view of Miura et al., Saito et al., Cole, Jr. et al. and Miyazawa et al., and therefore the claims were not properly rejected.

VII. CONCLUSION

For the foregoing reasons, Applicant respectfully requests that the rejection of all of the pending claims of the application be reversed.

January 3, 2007

Respectfully submitted,



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APPENDIX OF THE CLAIMS INVOLVED IN THE APPEAL

Claims 1 – 16 (cancelled).

Claim 17. A multi-layer printed circuit board having at least one prefabricated integrated electronic component embedded therein comprising:

a polymeric circuit board substrate comprising the core of said multi-layer printed circuit board and having a first substrate surface and a second substrate surface;

a first integrated electronic component, where said first integrated electronic component is prefabricated prior to being securely attached in a cavity in said first substrate surface;

a first dielectric layer disposed on said first substrate surface and over said first integrated electronic component;

a metallic layer disposed on said first dielectric layer;

an electrically conductive first via passing through said first dielectric layer in contact with said metallic layer; and

a second dielectric layer disposed over said first via and over said metallic layer,

a second electrically conductive via extending at one location through said first and second dielectric layers and electrically coupled to said first integrated electronic component.

Claim 18. The multi-layer printed circuit board of Claim 17 additionally comprising a first metallic layer disposed on said first substrate surface and a second metallic layer disposed on said second substrate surface.

Claim 19. The multilayer printed circuit board of Claim 17 wherein said circuit board substrate comprises a multi-layer core substrate comprising at least two polymeric layers.

Claim 20. The multilayer printed circuit board of Claim 17 wherein said first via extends from said first substrate surface to said second substrate surface.

Claim 21. The multilayer printed circuit board of Claim 18 wherein said first via extends from said first substrate surface to said second substrate surface.

Claim 22. The multilayer printed circuit board of Claim 18 wherein said first metallic layer is patterned to expose a portion of said first substrate surface, and said cavity is formed in the exposed portion of said first substrate surface.

Claim 23. The multilayer printed circuit board of Claim 18 wherein said second metallic layer is patterned to expose a portion of said second substrate surface.

Claim 24. The multilayer printed circuit board of Claim 23 additionally comprising a second integrated electronic component secured to said exposed portion of said second substrate surface.

Claim 25 (cancelled).

Claim 26. The multilayer printed circuit board of Claim 24 wherein said second integrated electronic component is disposed in a cavity formed in said exposed portion of said second substrate surface.

Claim 27. The multilayer printed circuit board of Claim 18 wherein said first prefabricated integrated electronic component comprises a conductive pad contacting said first metallic layer.

Claim 28. The multilayer printed circuit board of Claim 24 wherein said second integrated electronic component comprises a conductive pad contacting said second metallic layer.

Claim 29. The multilayer printed circuit board of Claim 26 wherein said first prefabricated integrated electronic component comprises a conductive pad contacting said first metallic layer.

Claim 30. The multilayer printed circuit board of Claim 17 additionally comprising at least one metal-lined via extending through said metallic layer and through said first dielectric layer.

Claim 31. The multilayer printed circuit board of Claim 24 additionally comprising at least one metal-lined via extending through said metallic layer and through said first dielectric layer.

Claim 32. The multilayer printed circuit board of Claim 26 additionally comprising at least one metal-lined via extending through said metallic layer and through said first dielectric layer.

Claim 33. The multilayer printed circuit board of Claim 27 additionally comprising at least one metal-lined via extending through said metallic layer and through said first dielectric layer.

Claim 34. The multilayer printed circuit board of Claim 33 additionally comprising a patterned metal layer disposed on said second dielectric layer.

Claim 35 (cancelled).

Claim 36. The multilayer printed circuit board of Claim 17 wherein said first prefabricated integrated electronic component is a capacitor.

Claim 37. The multilayer printed circuit board of Claim 36 wherein said capacitor comprises a petrovskite capacitance material.

Claim 38. The multilayer printed circuit board of Claim 17 wherein said first prefabricated integrated electronic component is fabricated at a temperature higher than the maximum processing temperature of the printed circuit board.

Claim 39. The multilayer printed circuit board of Claim 38 wherein said first prefabricated integrated electronic component is fabricated at a temperature of greater than about 600°C.

Claim 40. A multi-layer printed circuit board comprising:

a polymeric circuit board substrate comprising the core of said multi-layer printed circuit board;

a prefabricated capacitor disposed in a cavity in said substrate, said capacitor having a contact pad;

a first dielectric layer disposed on said substrate and over said capacitor;

a metallic layer disposed on said first dielectric layer;

an electrically conductive first via passing through said first dielectric layer in contact with said contact pad; and

a second dielectric layer disposed over said first via and over said metallic layer,

a second electrically conductive via extending at one location through said first and second dielectric layers and electrically coupled to said capacitor.

Claim 41. The multi-layer printed circuit board of claim 40, comprising a plurality of cavities and a plurality of capacitors.

Claim 42. The multi-layer printed circuit board of claim 40 wherein said capacitor comprises a petrovskite capacitance material.

Claim 43. The multi-layer printed circuit board of claim 40 wherein said capacitor is fabricated at a temperature higher than the maximum processing temperature of the printed circuit board.

Claim 44. A multi-layer printed circuit board comprising:

a polymeric circuit board substrate comprising the core of said multi-layer printed circuit board, said substrate having opposing first and second sides;

a prefabricated electronic component disposed in a cavity formed in said first side of said substrate, said prefabricated electronic component having a contact pad;

a first dielectric layer disposed on said first side of said substrate and over said prefabricated electronic component;

a patterned metallic layer disposed on said first dielectric layer;

an electrically conductive first via passing through said first dielectric layer in contact with said contact pad;

a second dielectric layer disposed over said first via and over said metallic layer;

a second electrically conductive via extending at one location through said first and second dielectric layers;

a third dielectric layer disposed on said second side of said substrate; and

a patterned metallic layer disposed on said third dielectric layer.

APPENDIX OF EVIDENCE

None.

APPENDIX OF RELATED PROCEEDINGS

None.